



# 12-Bit Successive Approximation High Accuracy A/D Converters

ANALOG DEVICES INC

**AD5210 Series**

### 1.1 Scope.

This specification covers the detail requirements for hybrid, 12-bit, successive approximation, high accuracy, analog-to-digital converters.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
±5V Ext Ref -12	AD5214TD/883B
±10V Int Ref -13	AD5212TD/883B
±10V Ext Ref -14	AD5215TD/883B

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000:

Device Type	Package Outline
-12	DH-24E
-13, -14	

### 1.3 Absolute Maximum Ratings. ( $T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage ( $+V_{CC}$ )	+18V
Negative Supply Voltage ( $-V_{EE}$ )	-18V
Logic Supply Voltage ( $+V_{DD}$ )	+7V
Analog Input Voltage	±25V
Digital Input Voltage	+5.5V
Reference Input Voltage (Ext. Ref versions only)	0 to -15V
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C
Junction Temperature	+175°C

### 1.5 Thermal Characteristics.

Thermal Resistance  $\theta_{JC} = 5^\circ\text{C}/\text{W}$   
 $\theta_{JA} = 40^\circ\text{C}/\text{W}$

Table 1.

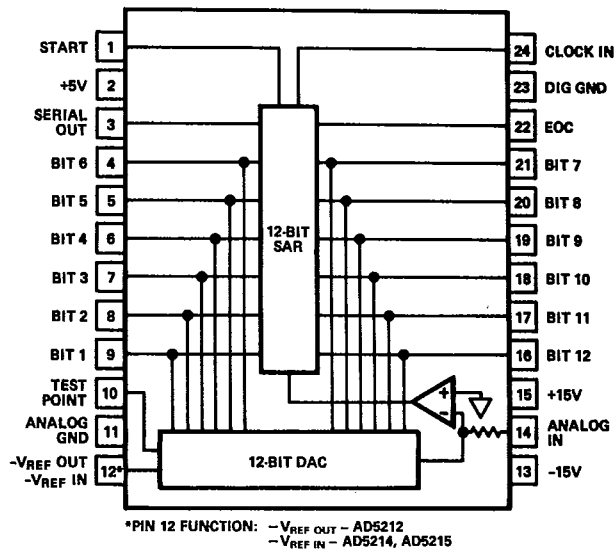
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1</sup>	Units
Analog Input Voltage	V <sub>IN</sub>	-12	±5				Ext. -10.000 V <sub>REF</sub>	VFS
	V <sub>IN</sub>	-13	±10				Internal Reference	VFS
		-14					Ext. -10.000 V <sub>REF</sub>	
Linearity Error	L <sub>E</sub>	All	1/2	1/2	1/2	At Major Carries (Abbreviated Test)	±LSB max	
Differential Linearity Error <sup>2</sup>	DNL	All	0.9	0.9	0.9	At Major Carries	±LSB max	
Zero Error	Z <sub>E</sub>	All	1	1	2	V <sub>IN</sub> = 0V	±LSB max	
±FS Absolute Accuracy Error Over Temperature	TC <sub>AE</sub>	-13	0.4		0.4		With Internal Reference	±%FSR max
		-12, 14	0.1		0.1		With Ext. -10.000 V <sub>REF</sub>	±%FSR max
±FS Absolute Accuracy Error @ +25°C	A <sub>E</sub>	All	2	2		With Ext. -10.000 V <sub>REF</sub> on Ext. Ref. Versions	±LSB max	
Conversion Time	t <sub>CONV</sub>	All	13	13		With 1MHz Clock	µs max	
Serial/Parallel Code Error Match	SP <sub>CM</sub>	All	0	0		Random	±Bits	
Logic Inputs	I <sub>INL</sub> I <sub>INH</sub> I <sub>INH</sub>	All	0.6 0.04 1.0	0.6 0.04 1.0		V <sub>INL</sub> = 0.3V V <sub>INH</sub> = 2.4V V <sub>INH</sub> = 5.5V	mA max	
Logic Outputs	V <sub>OL</sub> V <sub>OH</sub>		0.4 2.4	0.4 2.4		I <sub>OL</sub> = 3.2mA I <sub>OH</sub> = -80µA	V max V min	
Short Circuit Current	I <sub>SC</sub>		16	16		@ 0V	mA min	
Clock Input Pulse Width	t <sub>CW</sub>	All	100	100			ns min	
Power Supply Rejection	PSRR	All	0.005			0.005	All Supplies ±3% Variation	%/ % max
Power Supply Current	I <sub>CC</sub>	All	28	28				mA max
	I <sub>EE</sub>		35	35				
	I <sub>LOGIC</sub>		68	68				
Power Supplies	V <sub>CC</sub> V <sub>EE</sub> V <sub>LOGIC</sub>	All	+15 ±10% -15 ±10% +5 ±10%				V	
Power Dissipation	PD	-12, 14	0.8			0.8		Watts max
		-13	1.0			1.0		

**NOTES**
<sup>1</sup>T<sub>A</sub> = +25°C, V<sub>CC</sub> = ±15V, V<sub>DD</sub> = +5V unless otherwise noted.

<sup>2</sup>Guaranteed no missing codes.

3.2.1 Functional Block Diagram and Terminal Assignments.

Top View

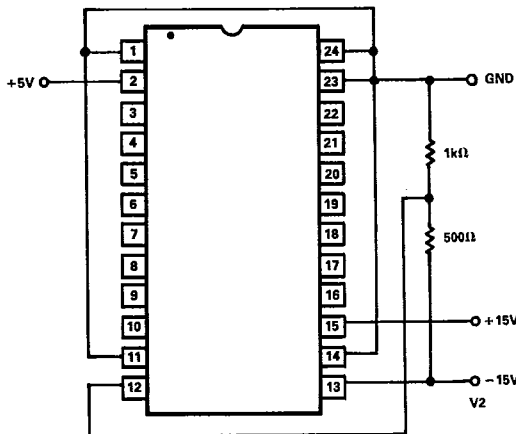


3.2.4 Microcircuit Technology Group.

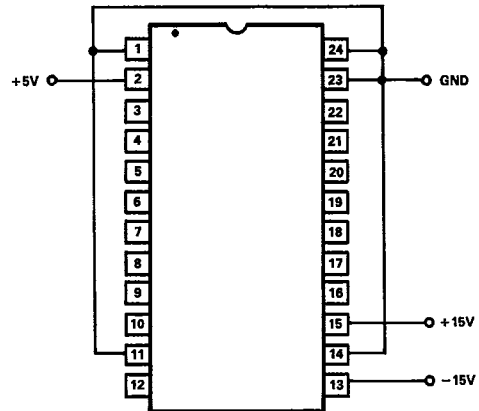
This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



Devices 12, 14



Device 13

## 6.0 Input Range.

The analog input range for each device is specified in Table 1.

## 6.1 Digital Output Data.

Both parallel and serial data from TTL storage registers are in negative true form using complementary offset binary (COB) coding. Parallel data becomes valid approximately 40ns after the EOC STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked 40ns after the "1" to "0" transition of the EOC STATUS flag on pin 22. Serial data coding is also complementary offset binary (COB) coding. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges and bit decisions are made on following rising clock edges. Serial data is guaranteed valid 200ns after the bit decision, permitting serial data to be clocked directly into a receiving register on the following falling clock edge, if it occurs 200ns after the rising edge. There are 13 negative-going clock edges in the complete 12-bit conversion cycle. Using a 12-bit serial input register, the first edge shifts in an invalid bit into the register, which is shifted out on the 13th negative going clock edge. The digital output codes corresponding to analog input voltage for calibration and test are shown in Table 2 below.

Table 2. Logic Coding (Complementary Offset Binary)

Device 12	Device 13, 14	MSB	LSB
+ 5.0000V	+ 10.000V	0	0
0.0000V	0.000V	1	0
- 4.9976V	- 9.995V	1	1

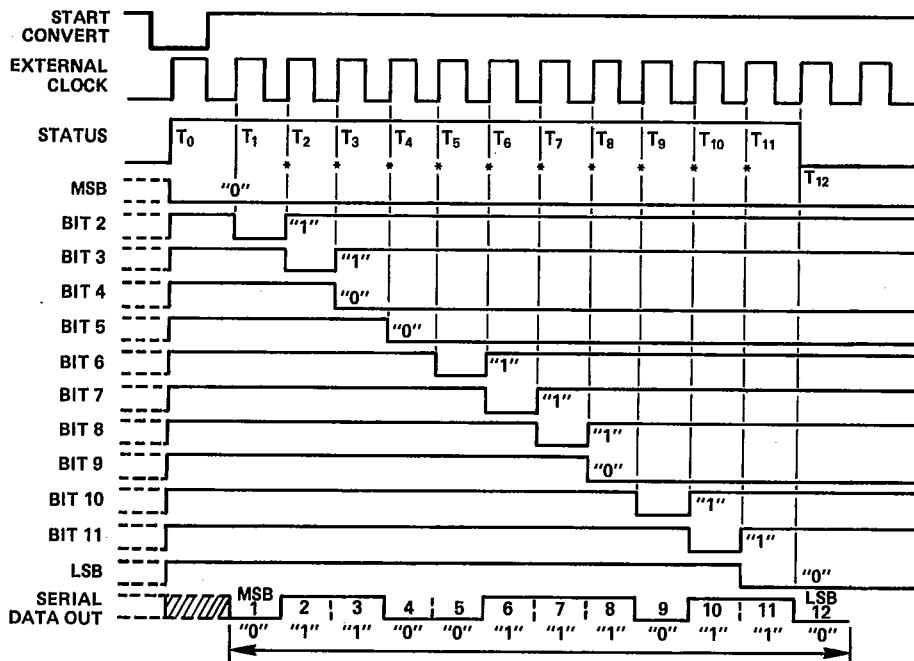


Figure 1. Timing Diagram